深圳市希恩凯电子有限公司
SHENZHEN CNK ELECTRONIC CO.,LTD.

Product Specification For LCD Module

Model NO.：CNKO0960-18225B1-W

CUSTOMERITEM NO.：

REVISION：A

☐APPROVAL FOR SPECIFICATIONS ONLY

■ **APPROVAL FOR SPECIFICATIONS AND SAMPLE**

CUSTOMER：	APPROVED BY：

CNK LCM R&D CENTER

APPROVED BY	CHECKED BY	PREPARED BY
DIRECTOR	MANAGER	Engineer

深圳市希恩凯电子有限公司
SHEN ZHEN CNK ELECTRONICS CO.,LTD
地 址： 惠州市惠阳区西湖村铭仕工业园 2 栋 1-2 楼
电 话： 0752-3556001
传 真： 0752-3556004

http://www.szcnk.com

PRODUCT CONTENTS

REVISION HISTORY

Rev.	Contents	Date

■ PHYSICAL DATA

No.	Items:	Specification:	Unit
1	Diagonal Size	0.96	Inch
2	Resolution	128(H) x 64(V)	Dots
3	Active Area	21.740(W) x 11.175(H)	mm^2
4	Outline Dimension (Panel)	26.70(W) x 19.26(H)	mm^2
5	Pixel Pitch	0.170(W) x 0.175(H)	mm^2
6	Pixel Size	0.150(W) x 0.150(H)	mm^2
7	Driver IC	SSD1306BZ	-
8	Display Color	White	-
9	Gray scale	1	Bit
10	Interface	Parallel/Serial/IIC	-
11	IC package type	COG	-
12	Thickness	(1.55)	mm
13	Weight	TBD	g
14	Duty	1/64	-

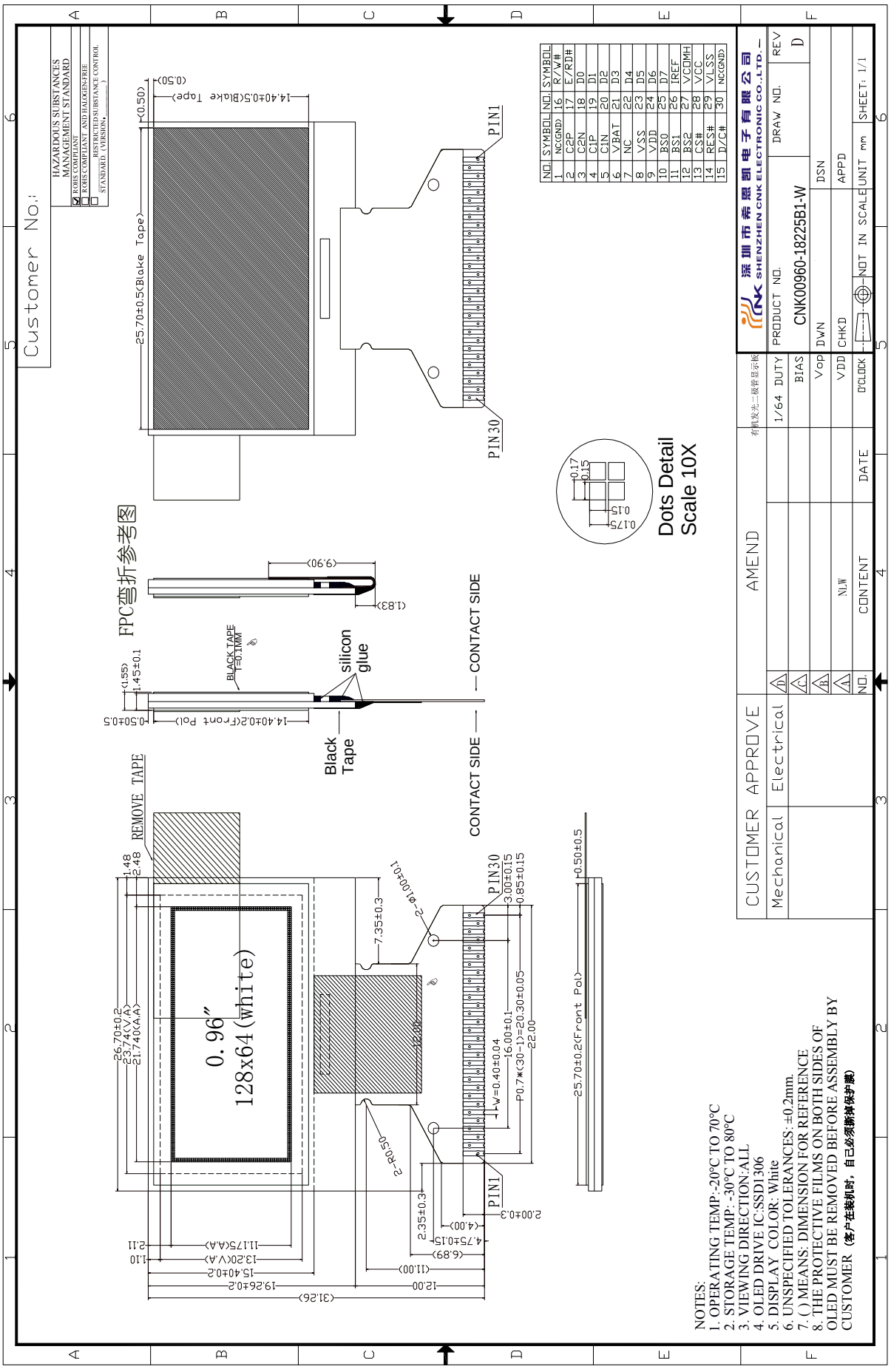
■ ABSOLUTE MAXIMUM RATINGS

Unless otherwise specified,(Voltage Referenced to V_{SS}) (Ta = 25℃)

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	-0.3	-	4.0	V
	Logic	V_{BAT}	-0.3		5.0	V
	Driving	V_{CC}	0	-	16.0	V
Operating Temperature		Top	-20	-	70	℃
Storage Temperature		Tst	-30	-	80	℃
Humidity		-	-	-	90	%RH

NOTE:
Permanent device damage may occur if **ABSOLUTE MAXIMUM RATINGS** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ EXTERNAL DIMENSIONS



■ ELECTRICAL CHARACTERISTICS

◆DC Characteristics

Condition(Unless otherwise specified): Voltage referenced to V_{SS}； V_{DD}=1.65V to 3.3V； Ta = 25℃

Items		Symbol	Min	Typ.	Max	Unit
Supply Voltage	Logic	V_{DD}	1.65	3.0	3.3	V
	Charge Pump Regulator Supply Voltage	V_{BAT}	2.2	-	4.2	V
	Operating	V_{CC}	7.0	9.0	15.0	V
Input Voltage	High Voltage	V_{IH}	0.8 x V_{DD}	-	-	V
	Low Voltage	V_{IL}	-	-	0.2 x V_{DD}	V
Output Voltage	High Voltage	V_{OH}	0.9 x V_{DD}	-	-	V
	Low Voltage	V_{OL}	-	-	0.1 x V_{DD}	V

◆AC Characteristics

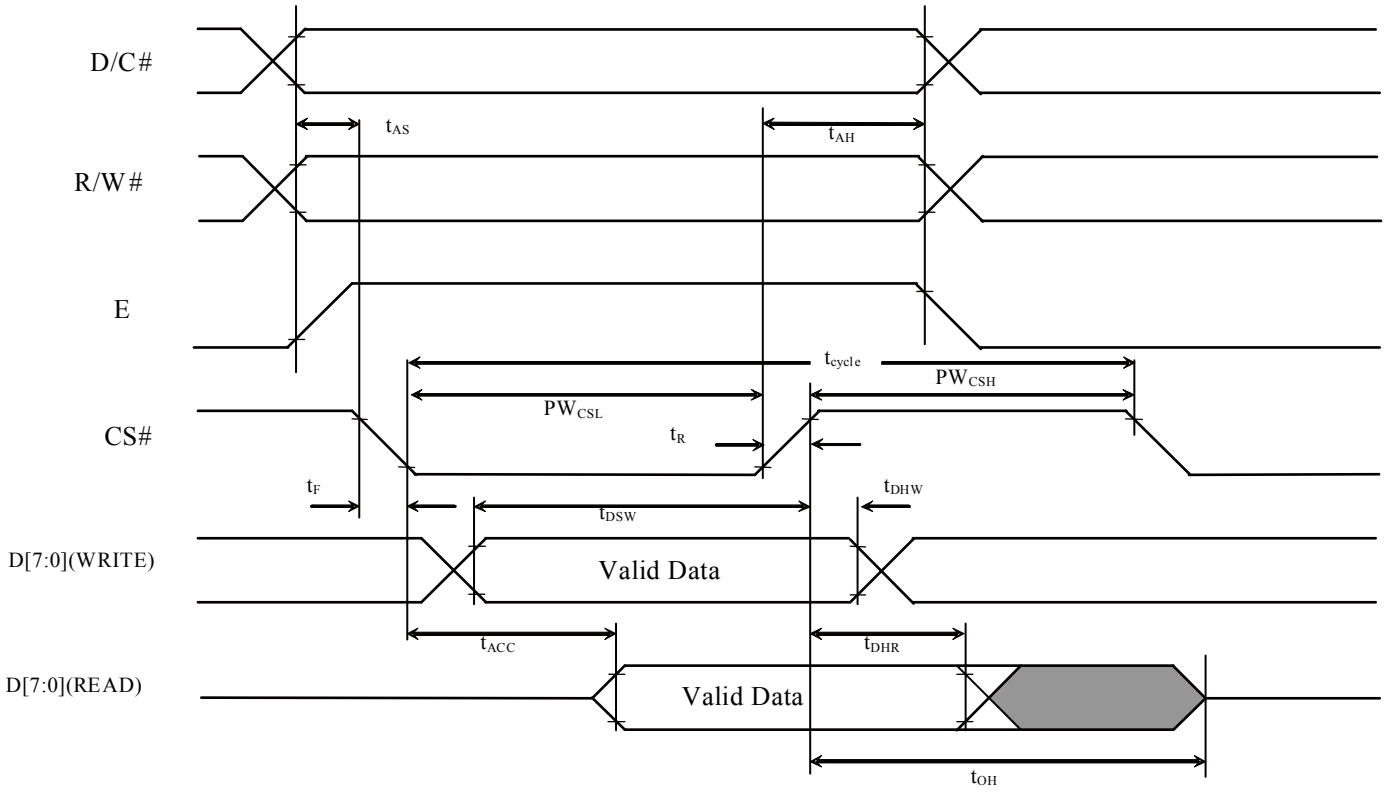
1. 6800 Series MPU Parallel Interface Timing Characteristics

6800-Series MCU Parallel Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	5	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

6800-series MCU parallel interface characteristics



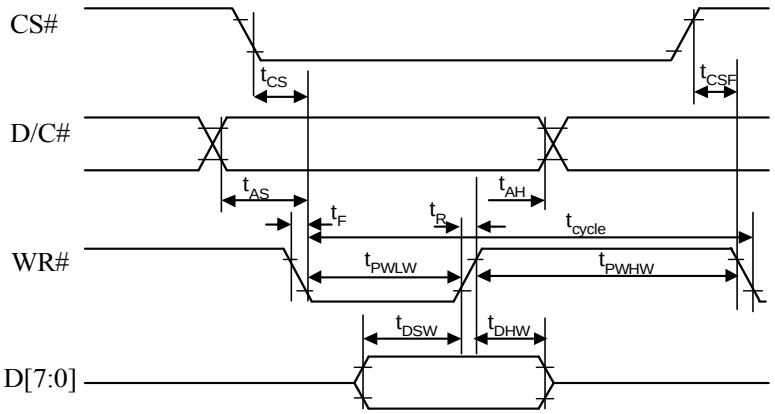
2. 8080 Series MPU Parallel Interface Timing Characteristics

(V_{DD}–V_{SS}=1.65V to 3.3V , T_A =25℃)

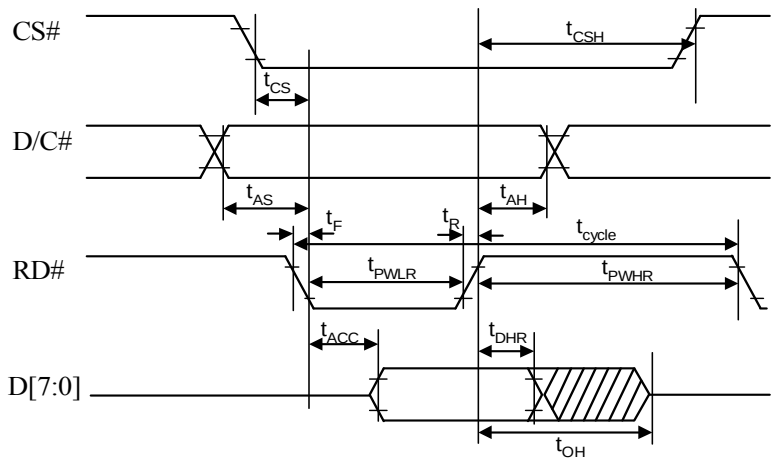
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	10	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
t_{PWLR}	Read Low Time	120	-	-	ns
t_{PWLW}	Write Low Time	60	-	-	ns
t_{PWHR}	Read High Time	60	-	-	ns
t_{PWHW}	Write High Time	60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns
t_{CS}	Chip select setup time	0	-	-	ns
t_{CSH}	Chip select hold time to read signal	0	-	-	ns
t_{CSF}	Chip select hold time	20	-	-	ns

8080-series parallel interface characteristics

Write Cycle



Read cycle

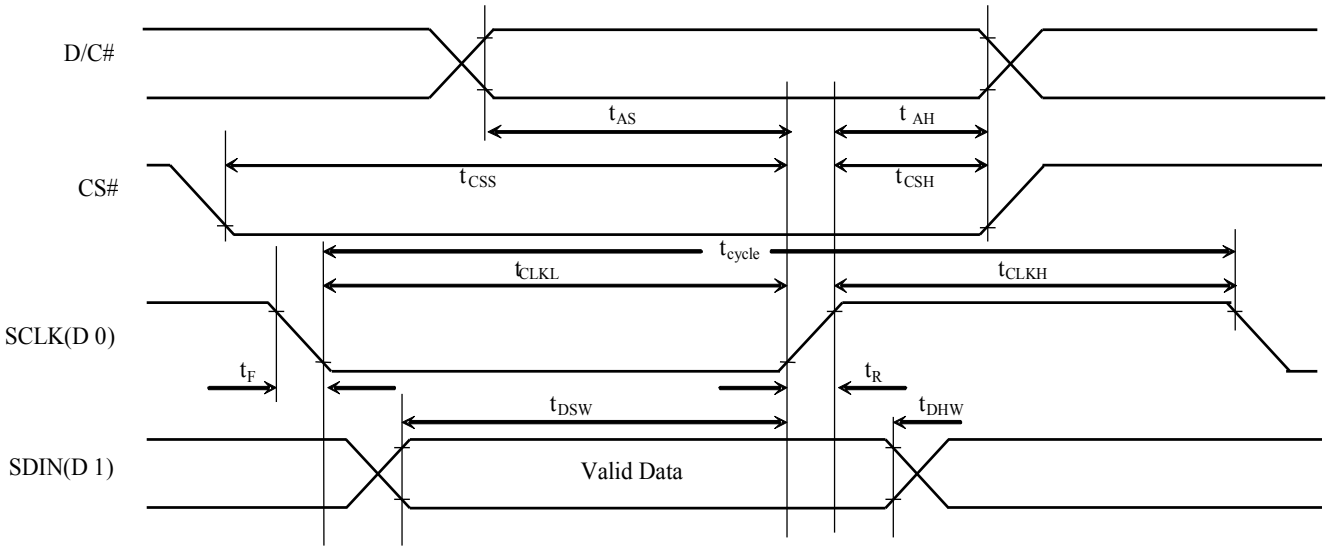


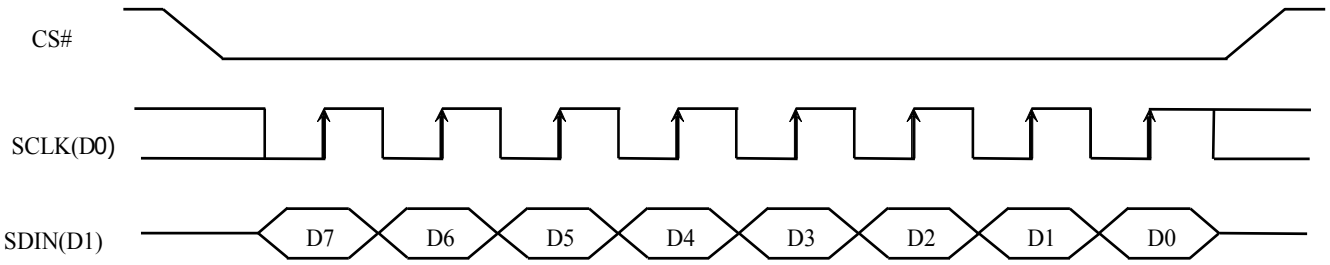
3. 4-wire Serial Interface Timing Characteristics

(V_{DD} – V_{SS}=1.65V to 3.3V , T_A =25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	15	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

4-wire Serial interface characteristics





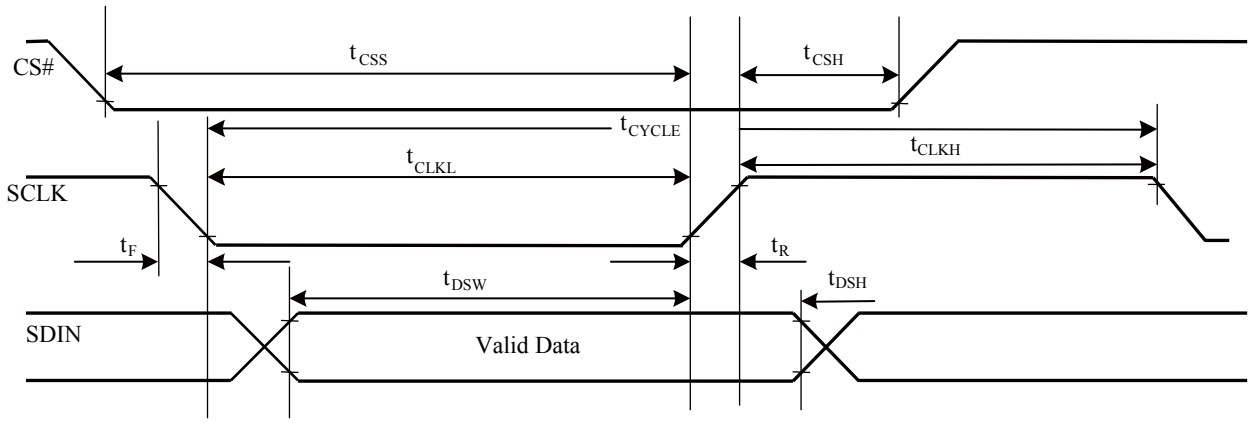
4. 3-wire Serial Interface Timing Characteristics

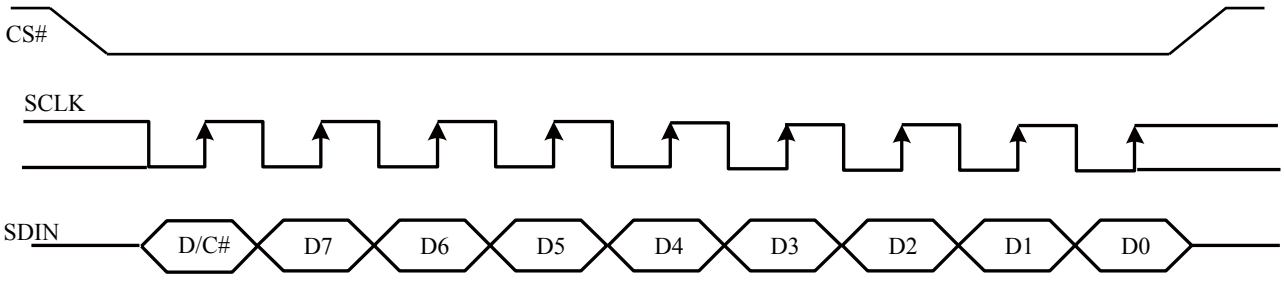
3-wire Serial Interface Timing Characteristics

(V_{DD} - V_{SS} = 1.65V to 3.3V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	100	-	-	ns
t_{CSS}	Chip Select Setup Time	20	-	-	ns
t_{CSH}	Chip Select Hold Time	10	-	-	ns
t_{DSW}	Write Data Setup Time	15	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	20	-	-	ns
t_{CLKH}	Clock High Time	20	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

3-wire Serial interface characteristics



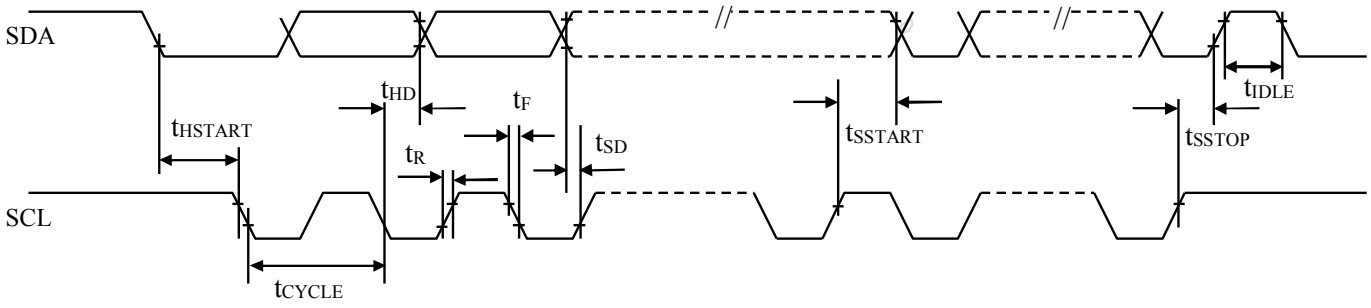


5. I² C Interface Timing Characteristics:

(V_{DD} – V_{SS}=1.65V to 3.3V , T_A=25℃)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{HD}	Data Hold Time (for "SDA_{OUT}" pin)	0	-	-	ns
	Data Hold Time (for "SDA_{IN}" pin)	300	-	-	ns
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_F	Fall Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I² C interface Timing characteristics



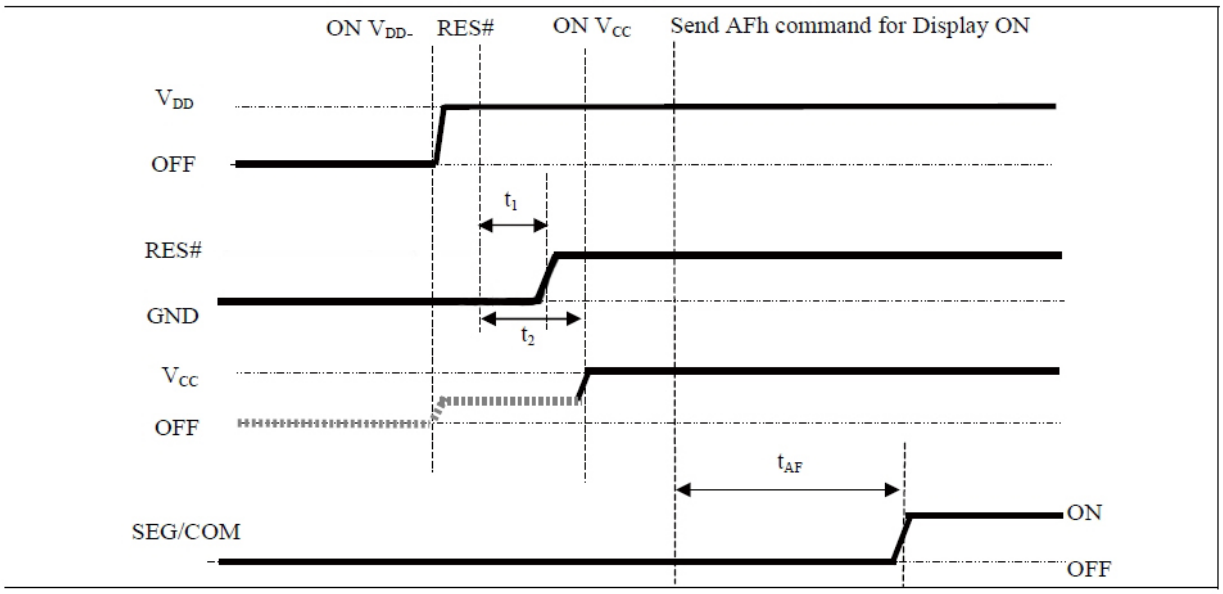
■ TIMING OF POWER SUPPLY

Power ON and OFF sequence with External V_{CC}

Power ON sequence:

1. Power ON V_{DD}
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [4] and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then Power ON V_{CC}.[1]
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms (t_{AF}).

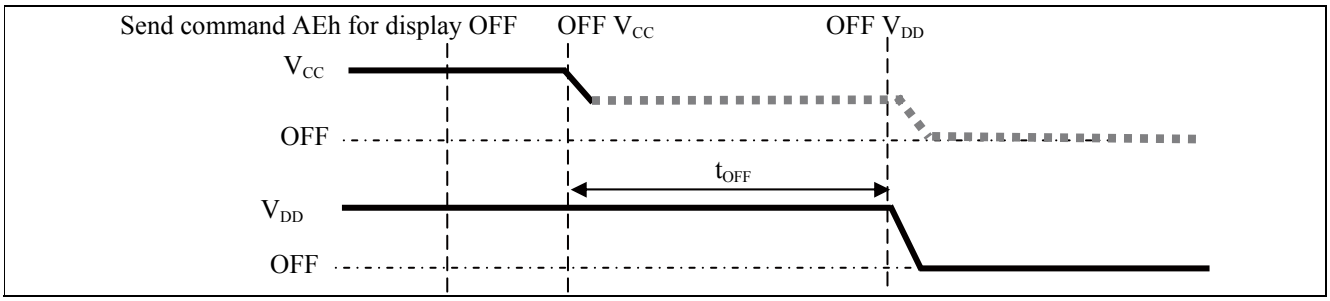
The Power ON sequence



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}.[1], [2], [3]
3. Power OFF V_{DD} after t_{OFF}. [5] (Typical t_{OFF}=100ms)

The Power OFF sequence



Note:

[1] Since an ESD protection circuit is connected between V_{DD} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in Figure 8-16 and Figure 8-17.

[2] V_{CC} should be kept float (i.e. disable) when it is OFF.

[3] Power Pins (V_{DD} , V_{CC}) can never be pulled to ground under any circumstance.

[4] The register values are reset after t_1.

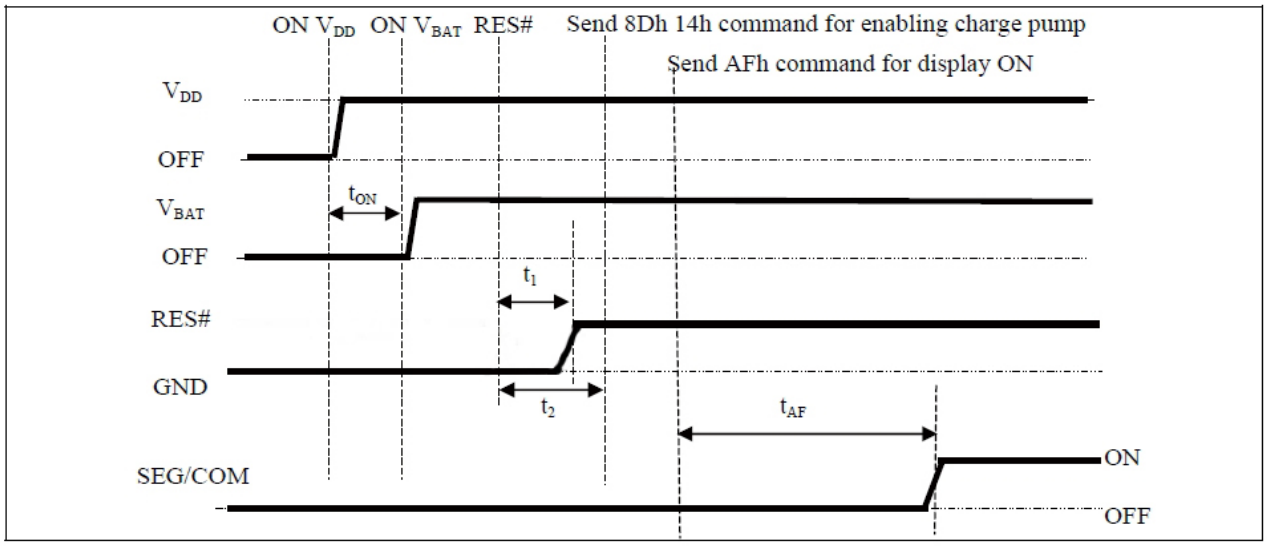
[5] V_{DD} should not be Power OFF before V_{CC} Power OFF.

Power ON and OFF sequence with Charge Pump Application

Power ON sequence:

1. Power ON V_{DD}
2. Wait for t_{ON}. Power ON V_{BAT}. [1], [2] (where Minimum t_{ON} = 0ms)
3. After V_{BAT} become stable, set RES# pin LOW (logic low) for at least 3us (t_1) [3] and then HIGH (logic high).
4. After set RES# pin LOW (logic low), wait for at least 3us (t_2). Then input commands with below sequence:
   a. 8Dh 14h for enabling charge pump
   b. AFh for display ON
5. SEG/COM will be ON after 100ms (t_{AF}).

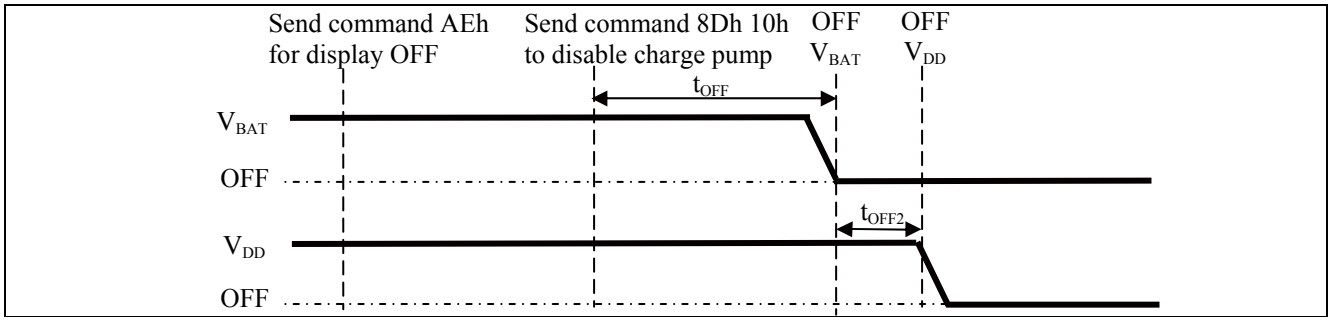
The Power ON sequence with Charge Pump Application



Power OFF sequence:

1. Send command AEh for display OFF
2. Send command 8Dh 10h to disable charge pump
3. Power OFF V_{BAT} after t_{OFF}. [1], [2] (Typical t_{OFF} =100ms)
4. Power OFF V_{DD} after t_{OFF2}. (where Minimum t_{OFF2} = 0ms [4] , Typical t_{OFF2}=5ms)

The Power OFF sequence with Charge Pump Application



Note:

[1] V_{BAT} should be kept float (i.e. disable) when it is OFF.
[2] Power Pins (V_{DD} , V_{BAT}) can never be pulled to ground under any circumstance.
[3] The register values are reset after t_1.
[4] V_{DD} should not be Power OFF before V_{BAT} Power OFF

■ ELECTRO-OPTICAL CHARACTERISTICS (Ta=25℃)

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Operating Luminance		L	70	90	-	cd /m^2	All pixels ON
Power Consumption		P	-	30	45	mW	30% pixels ON
Frame Frequency		Fr	-	100	-	Hz	-
Color Coordinate	White	CIE x	0.22	0.26	0.30	CIE1931	Darkroom
		CIE y	0.25	0.29	0.33		
Response Time	Rise	Tr	-	-	0.02	ms	-
	Decay	Td	-	-	0.02	ms	-
Contrast Ratio*		Cr	10000:1	-	-	-	Darkroom
Viewing Angle Uniformity		△ θ	160	-	-	Degree	-
Operating Life Time*		Top	24,000	-	-	Hours	L=90cd/m^2

Note:

1. 90cd/m2 is based on VDD=3.0V， VCC=9.0V， contrast command setting 0x80;

2. **Contrast ratio** is defined as follows:

$$\text{Contrast ratio} = \frac{\text{Photo – detector output with OLED being “white”}}{\text{Photo – detector output with OLED being “black”}}$$

3. **Life Time** is defined when the Luminance has decayed to less than 50% of the initial Luminance specification. (Odd and even chess board alternately displayed)
(The initial value should be closed to the typical value after adjusting.)

■ INTERFACE PIN CONNECTIONS

No.	Symbol	Description
1	NC(GND)	No connection.
2	C2P	C1P/C1N-Pin for charge pump capacitor; Connect to each other with a capacitor. C2P/C2N-Pin for charge pump capacitor; Connect to each other with a capacitor.
3	C2N	
4	C1P	
5	C1N	
6	VBAT	Power supply for charge pump regulator circuit.
7	NC	No connection.
8	VSS	This is a ground pin.
9	VDD	Power supply pin for core logic operation.
10	BS0	MCU bus interface selection pins. Please refer the table below for the details of setting.
11	BS1	
12	BS2	
13	CS#	This is the chip select input.(active LOW).
14	RES#	Reset signal input. When the pin is pulled LOW, initialization of the chip is excute. Keep this pin HIGH(i.e connect to VDD)during normal operation
15	D/C#	This is Data/Command control pin. When it is pulled HIGH (i.e. connect to VDD), the data at D[7:0] is treated as data. When it is pulled LOW, the data at D[7:0] will be transferred to the command register. In I2C mode, this pin acts as SA0 for slave address selection. When 3-wire serial interface is selected, this pin must be connected to VSS.
16	R/W#	This is read / write control input pin connecting to the MCU interface. When interfacing to a 6800-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Read mode will be carried out when this pin is pulled HIGH (i.e. connect to VDD) and write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.

17	E/RD#	When interfacing to a 6800-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled HIGH (i.e. connect to VDD) and the chip is selected. When connecting to an 8080-series microprocessor, this pin receives the Read (RD#) signal. Read operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I2C interface is selected, this pin must be connected to VSS.
18 - 25	D0-D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 will be the serial data input: SDIN and D2 should be kept NC. When I2C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
26	IREF	This is segment output current reference pin. A resistor should be connected between this pin and VSS to maintain the IREF current at 12.5 uA.
27	VCOMH	The pin for COM signal deselected voltage level. A capacitor should be connected between this pin and VSS.
28	VCC	Power supply for panel driving voltage. This is also the most positive power voltage supply pin. When charge pump is enabled, a capacitor should be connected between this pin and VSS.
29	VLSS	This is an analog ground pin. It should be connected to VSS externally.
30	NC(GND)	No connection

MCU Bus Interface Pin Selection

SSD1306 Pin Name	I^2C Interface	6800-parallel interface (8 bit)	8080-parallel interface(8 bit)	4-wire Serial interface	3-wire Serial interface
BS0	0	0	0	0	1
BS1	1	0	1	0	0
BS2	0	1	1	0	0

Note
(1) 0 is connected to V_{SS}
(2) 1 is connected to V_{DD}

Status	V_{BAT}	V_{DD}	V_{CC}
Enable Charge pump	Connect to external VBAT source	Connect to external VDD source	A capacitor should be connected between this pin and VSS
Disable Charge pump	Keep float	Connect to external VDD source	Connect to external VCC source

■ COMMAND TABLE

(D/C#=0, R/W#(WR#) = 0, E(RD#=1) unless specific setting is stated)

1. Fundamental Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	81 A[7:0]	1 A_7	0 A_6	0 A_5	0 A_4	0 A_3	0 A_2	0 A_1	1 A_0	Set Contrast Control	Double byte command to select one of the contrast steps. Contrast increases as the value increases. (RESET = 7Fh) A[7:0] valid range: 01h to FFh
0	A4/A5	1	0	1	0	0	1	0	X_0	Entire Display ON	A4h, X_0=0b: Resume to RAM content display (RESET) Output follows RAM content A5h, X_0=1b: Entire display ON Output ignores RAM content
0	A6/A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display	A6h, X[0]=0b: Normal display (RESET) 0 in RAM: OFF in display panel 1 in RAM: ON in display panel A7h, X[0]=1b: Inverse display 0 in RAM: ON in display panel 1 in RAM: OFF in display panel
0	AD	1	0	1	0	1	1	0	1	Internal I_{REF} Setting	Select external or internal I_{REF} : A[4] = '0': Select external I_{REF} (RESET) A[4] = '1': Enable internal I_{REF} during display ON Internal I_{REF} value setting: A[5] = '0': Internal I_{REF} setting: 19uA, output a maximum I_{SEG}=150uA (RESET) A[5] = '1': Internal I_{REF} setting: 30uA, output a maximum I_{SEG}=240uA Note (1) Refer to section 7.8 for details.
0	A[5:4]	0	0	A_5	A_4	0	0	0	0		
0	AE/AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF	AEh, X[0]=0b:Display OFF (sleep mode) (RESET) AFh X[0]=1b:Display ON in normal mode
0	E3	1	1	1	0	0	0	1	1	NOP	Command for no operation

2. **Scrolling Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	26/27	0	0	1	0	0	1	1	X_0	Continuous Horizontal Scroll Setup	26h, X[0]=0, Right Horizontal Scroll 27h, X[0]=1, Left Horizontal Scroll (Horizontal scroll by 1 column)
0	A[7:0]	0	0	0	0	0	0	0	0		
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		
0	C[2:0]	*	*	*	*	*	C_2	C_1	C_0		
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		
0	E[7:0]	*	E_6	E_5	E_4	E_3	E_2	E_1	E_0		
0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		

A[7:0] : Dummy byte (Set as 00h)

B[2:0] : Define start page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

C[2:0] : Set time interval between each scroll step in terms of frame frequency

000b – 6 frames	100b – 3 frames
001b – 32 frames	101b – 4 frames
010b – 64 frames	110b – 5 frame
011b – 128 frames	111b – 2 frame

D[2:0] : Define end page address

000b – PAGE0	011b – PAGE3	110b – PAGE6
001b – PAGE1	100b – PAGE4	111b – PAGE7
010b – PAGE2	101b – PAGE5	

E[6:0] : Define start column address (RESET = 00h)

F[6:0] : Define end column address (RESET = 7Fh)

Notes:

(1) The value of D[2:0] must be larger than or equal to B[2:0]

(2) The value of F[6:0] must be larger than or equal to E[6:0]

2. **Scrolling Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	29/2A	0	0	1	0	1	0	X_1	X_0	Continuous Vertical and Horizontal Scroll Setup	29h, X_1X_0=01b : Vertical and Right Horizontal Scroll 2Ah, X_1X_0=10b : Vertical and Left Horizontal Scroll (Horizontal scroll by 1 column) A[7:0] : Dummy byte B[2:0] : Define start page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | C[2:0] : Set time interval between each scroll step in terms of frame frequency 000b – 6 frames | 100b – 3 frames 001b – 32 frames | 101b – 4 frames 010b – 64 frames | 110b – 5 frame 011b – 128 frames | 111b – 2 frame D[2:0] : Define end page address 000b – PAGE0 | 011b – PAGE3 | 110b – PAGE6 001b – PAGE1 | 100b – PAGE4 | 111b – PAGE7 010b – PAGE2 | 101b – PAGE5 | The value of D[2:0] must be larger or equal to B[2:0] E[5:0] : Vertical scrolling offset e.g. E[5:0]= 01h refer to offset =1 row E[5:0] =3Fh refer to offset =63 rows **Note** (1) No continuous vertical scrolling is available.
0	2E	0	0	1	0	1	1	1	0	Deactivate scroll	Stop scrolling that is configured by command 26h/27h/29h/2Ah. **Note** (1) After sending 2Eh command to deactivate the scrolling action, the ram data needs to be rewritten.
0	2F	0	0	1	0	1	1	1	1	Activate scroll	Start scrolling that is configured by the scrolling setup

2. **Scrolling Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
											commands :26h/27h/29h/2Ah with the following valid sequences: Valid command sequence 1: 26h ;2Fh. Valid command sequence 2: 27h ;2Fh. Valid command sequence 3: 29h ;2Fh. Valid command sequence 4: 2Ah ;2Fh. For example, if "26h; 2Ah; 2Fh." commands are issued, the setting in the last scrolling setup command, i.e. 2Ah in this case, will be executed. In other words, setting in the last scrolling setup command overwrites the setting in the previous scrolling setup commands.
0 0 0	A3 A[5:0] B[6:0]	1 * *	0 * B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	1 A_1 B_1	1 A_0 B_0	Set Vertical Scroll Area	A[5:0] : Set No. of rows in top fixed area. The No. of rows in top fixed area is referenced to the top of the GDDRAM (i.e. row 0).[RESET = 0] B[6:0] : Set No. of rows in scroll area. This is the number of rows to be used for vertical scrolling. The scroll area starts in the first row below the top fixed area. [RESET = 64] **Note** (1) A[5:0]+B[6:0] <= MUX ratio (2) B[6:0] <= MUX ratio (3a) Vertical scrolling offset (E[5:0] in 29h/2Ah) < B[6:0] (3b) Set Display Start Line ($X_5X_4X_3X_2X_1X_0$ of 40h~7Fh) < B[6:0] (4) The last row of the scroll area shifts to the first row of the scroll area. (5) For 64d MUX display A[5:0] = 0, B[6:0]=64 : whole area scrolls A[5:0] = 0, B[6:0] < 64 : top area scrolls A[5:0] + B[6:0] < 64 : central area scrolls A[5:0] + B[6:0] = 64 : bottom area scrolls
0 0 0 0 0 0	2C/2D A[7:0] B[2:0] C[7:0] D[2:0] E[7:0]	0 0 * * * *	0 0 * * * E_6	1 0 * * * E_5	0 0 * * * E_4	1 0 * * * E_3	1 0 B_2 0 D_2 E_2	0 0 B_1 0 D_1 E_1	X_0 0 B_0 1 D_0 E_0	Content Scroll Setup	2Ch, X[0]=0, Right Horizontal Scroll by one column 2Dh, X[0]=1, Left Horizontal Scroll by one column A[7:0] : Dummy byte (Set as 00h) B[2:0] : Define start page address

2. Scrolling Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	F[7:0]	*	F_6	F_5	F_4	F_3	F_2	F_1	F_0		000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 C[7:0] : Dummy byte (Set as 01h) D[2:0] : Define end page address 000b – PAGE0 / 011b – PAGE3 / 110b – PAGE6 001b – PAGE1 / 100b – PAGE4 / 111b – PAGE7 010b – PAGE2 / 101b – PAGE5 E[6:0] : Define start column address (RESET = 00h) F[6:0] : Define end column address (RESET = 7Fh) **Note** (1) The value of D[2:0] must be larger than or equal to B[2:0] (2) The value of F[6:0] must be larger than E[6:0] (3) A delay time of 2 frame frequency must be set if sending the command of 2Ch / 2Dh consecutively

3. Addressing Setting Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Start Address for Page Addressing Mode	Set the lower nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Start Address for Page Addressing Mode	Set the higher nibble of the column start address register for Page Addressing Mode using X[3:0] as data bits. The initial display line register is reset to 0000b after RESET. **Note** (1) This command is only for page addressing mode
0 0	20 A[1:0]	0 *	0 *	1 *	0 *	0 *	0 *	0 A_1	0 A_0	Set Memory Addressing Mode	A[1:0] = 00b, Horizontal Addressing Mode A[1:0] = 01b, Vertical Addressing Mode A[1:0] = 10b, Page Addressing Mode (RESET) A[1:0] = 11b, Invalid
0 0 0	21 A[6:0] B[6:0]	0 * *	0 A_6 B_6	1 A_5 B_5	0 A_4 B_4	0 A_3 B_3	0 A_2 B_2	0 A_1 B_1	1 A_0 B_0	Set Column Address	Setup column start and end address A[6:0] : Column start address, range : 0-127d, (RESET=0d)

3. **Addressing Setting Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
											B[6:0]: Column end address, range : 0-127d, (RESET =127d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0 0 0	22 A[2:0] B[2:0]	0 * *	0 * *	1 * *	0 * *	0 * *	0 A_2 B_2	1 A_1 B_1	0 A_0 B_0	Set Page Address	Setup page start and end address A[2:0] : Page start Address, range : 0-7d, (RESET = 0d) B[2:0] : Page end Address, range : 0-7d, (RESET = 7d) **Note** (1) This command is only for horizontal or vertical addressing mode.
0	B0~B7	1	0	1	1	0	X_2	X_1	X_0	Set Page Start Address for Page Addressing Mode	Set GDDRAM Page Start Address (PAGE0~PAGE7) for Page Addressing Mode using X[2:0]. **Note** (1) This command is only for page addressing mode.

4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	40~7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000b during RESET.
0	A0/A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map	A0h, X[0]=0b: column address 0 is mapped to SEG0 (RESET) A1h, X[0]=1b: column address 127 is mapped to SEG0
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio	Set MUX ratio to N+1 MUX N=A[5:0] : from 16MUX to 64MUX, RESET= 111111b (i.e. 63d, 64MUX) A[5:0] from 0 to 14 are invalid entry.
0	C0/C8	1	1	0	0	X_3	0	0	0	Set COM Output Scan Direction	C0h, X[3]=0b: normal mode (RESET) Scan from COM0 to COM[N –1] C8h, X[3]=1b: remapped mode. Scan from COM[N-1] to COM0 Where N is the Multiplex ratio.

4. **Hardware Configuration (Panel resolution & layout related) Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	D3 A[5:0]	1 *	1 *	0 A_5	1 A_4	0 A_3	0 A_2	1 A_1	1 A_0	Set Display Offset	Set vertical shift by COM from 0d~63d The value is reset to 00h after RESET.
0 0	DA A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 1	0 0	Set COM Pins Hardware Configuration	A[4]=0b, Sequential COM pin configuration A[4]=1b(RESET), Alternative COM pin configuration A[5]=0b(RESET), Disable COM Left/Right remap A[5]=1b, Enable COM Left/Right remap

5. Timing & Driving Scheme Setting Command Table											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0 0	D5 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	0 A_3	1 A_2	0 A_1	1 A_0	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] : Define the divide ratio (D) of the display clocks (DCLK): Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] : Set the Oscillator Frequency, F_{OSC}. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 1000b Range:0000b~1111b. Frequency increases as setting value increases.
0 0	D9 A[7:0]	1 A_7	1 A_6	0 A_5	1 A_4	1 A_3	0 A_2	0 A_1	1 A_0	Set Pre-charge Period	A[3:0] : Phase 1 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h) A[7:4] : Phase 2 period of up to 15 DCLK clocks 0 is invalid entry (RESET=2h)
0 0	DB A[5:4]	1 0	1 0	0 A_5	1 A_4	1 0	0 0	1 0	1 0	Set V_{COMH} Deselect Level	A[5:4] / Hex code / V_{COMH} deselect level 00b / 00h / ~ 0.65 x V_{CC} 01b / 10h / ~ 0.71 x V_{CC} 10b / 20h / ~ 0.77 x V_{CC} (RESET) 11b / 30h / ~ 0.83 x V_{CC}

6. **Advance Graphic Command Table**											
D/C#	**Hex**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Command**	**Description**
0	23	0	0	1	0	0	0	1	1	Set Fade	A[5:4] = 00b Disable Fade Out / Blinking Mode[RESET]

6. **Advance Graphic Command Table**

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	A[6:0]	*	*	A5	A4	A3	A2	A1	A0	Out and Blinking	A[5:4] = 10b Enable Fade Out mode. Once Fade Mode is enabled, contrast decrease gradually to all pixels OFF. Output follows RAM content when Fade mode is disabled. A[5:4] = 11b Enable Blinking mode. Once Blinking Mode is enabled, contrast decrease gradually to all pixels OFF and than contrast increase gradually to normal display. This process loop continuously until the Blinking mode is disabled. A[3:0] : Set time interval for each fade step (1) A[3:0] / Time interval for each fade step: 0000b = 8 Frames; 0001b = 16 Frames; 0010b = 24 Frames; : ; 1111b = 128 Frames Refer to section 9.3.1 for details.
0 0	D6 A[0]	1 0	1 0	0 0	1 0	0 0	1 0	1 0	0 A0	Set Zoom In	A[0] = 0b Disable Zoom in Mode[RESET] A[0] = 1b Enable Zoom in Mode Note (1) The panel must be in alternative COM pin configuration (command DAh A[4] =1) (2) Refer to section 9.3.2 for details.

7. Charge Pump Command Table

D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0 0	8D A[7:0]	1 A_7	0 *	0 0	0 1	1 0	1 A_2	0 0	1 A_0	Charge Pump Setting	Enable / Disable internal charge pump: A[2] = 0b, Disable charge pump (RESET) A[2] = 1b, Enable charge pump during display on A[7] / A[0] / Hex code / Charge Pump Mode: 0b / 0b / 14h / 7.5V (RESET); 0b / 1b / 15h / 6.0V; 1b / 0b / 94h / 8.5V; 1b / 1b / 95h / 9.0V **Note** (1) The Charge Pump must be enabled by the following command sequence: 8Dh ; Charge Pump Setting 14h / 15h / 94h / 95h ; Enable Charge Pump AFh; Display ON

Note
(1) "*" stands for "Don't care".

■ INITIALIZATION CODE(External VCC)

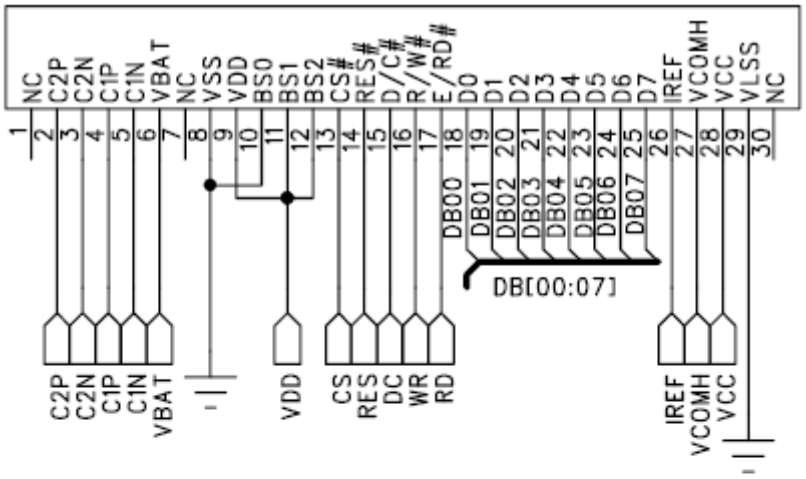
```
void Init_SSD1306(void)
{
    Write_Command(0xAE);            //Set Display Off

    Write_Command(0xD5);            //Display divide ratio/osc. freq. mode
    Write_Command(0x80);

    Write_Command(0xA8);            //Multiplex ration mode:63
    Write_Command(0x3F);

    Write_Command(0xD3);            //Set Display Offset
    Write_Command(0x00);

    Write_Command(0x40);            //Set Display Start Line

    Write_Command(0x8D);            //DC-DC Control Mode Set
    Write_Command(0x10);            //DC-DC ON/OFF Mode Set

    Write_Command(0xA0);            //Segment Remap

    Write_Command(0xC0);            //Set COM Output Scan Direction

    Write_Command(0xDA);            //Set COM Pins Hardware Configuration
    Write_Command(0x12);

    Write_Command(0x81);            //Contrast control
    Write_Command(CONTRAST);

    Write_Command(0xD9);            //Set pre-charge period
    Write_Command(0x22);

    Write_Command(0xDB);            //VCOM deselect level mode
    Write_Command(0x40);

    Write_Command(0xA4);            //Set Entire Display On/Off

    Write_Command(0xA6);            //Set Normal Display

    ClearRAM();

    Write_Command(0xAF);            //Set Display On
}
```

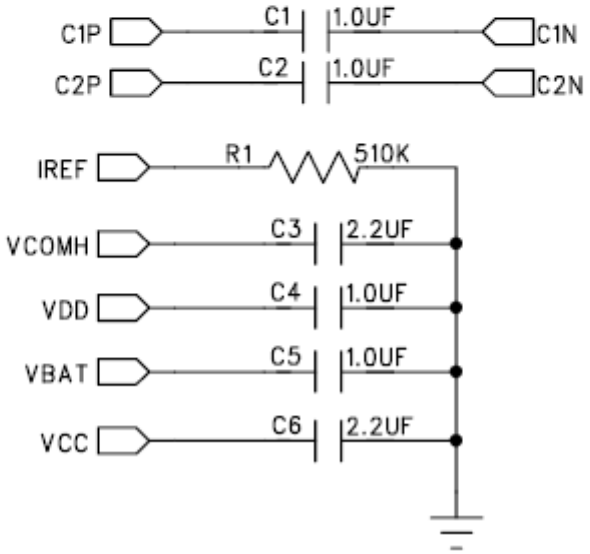
■ INITIALIZATION CODE(Internal VCC)

```
void Init_SSD1306(void)
{
    Write_Command(0xAE);            //Set Display Off

    Write_Command(0xD5);            //Display divide ratio/osc. freq. mode
    Write_Command(0x80);

    Write_Command(0xA8);            //Multiplex ration mode:63
    Write_Command(0x3F);

    Write_Command(0xD3);            //Set Display Offset
    Write_Command(0x00);

    Write_Command(0x40);            //Set Display Start Line

    Write_Command(0x8D);            //DC-DC Control Mode Set
    Write_Command(0x14);            //DC-DC ON/OFF Mode Set 7.5V

    Write_Command(0xA0);            //Segment Remap

    Write_Command(0xC0);            //Set COM Output Scan Direction

    Write_Command(0xDA);            //Set COM Pins Hardware Configuration
    Write_Command(0x12);

    Write_Command(0x81);            //Contrast control
    Write_Command(CONTRAST);

    Write_Command(0xD9);            //Set pre-charge period
    Write_Command(0x22);

    Write_Command(0xDB);            //VCOM deselect level mode
    Write_Command(0x40);

    Write_Command(0xA4);            //Set Entire Display On/Off

    Write_Command(0xA6);            //Set Normal Display

    ClearRAM();

    Write_Command(0xAF);            //Set Display On
}
```

■ SCHEMATIC EXAMPLE

◆8080 Series Interface Application Circuit(With Internal Charge Pump):





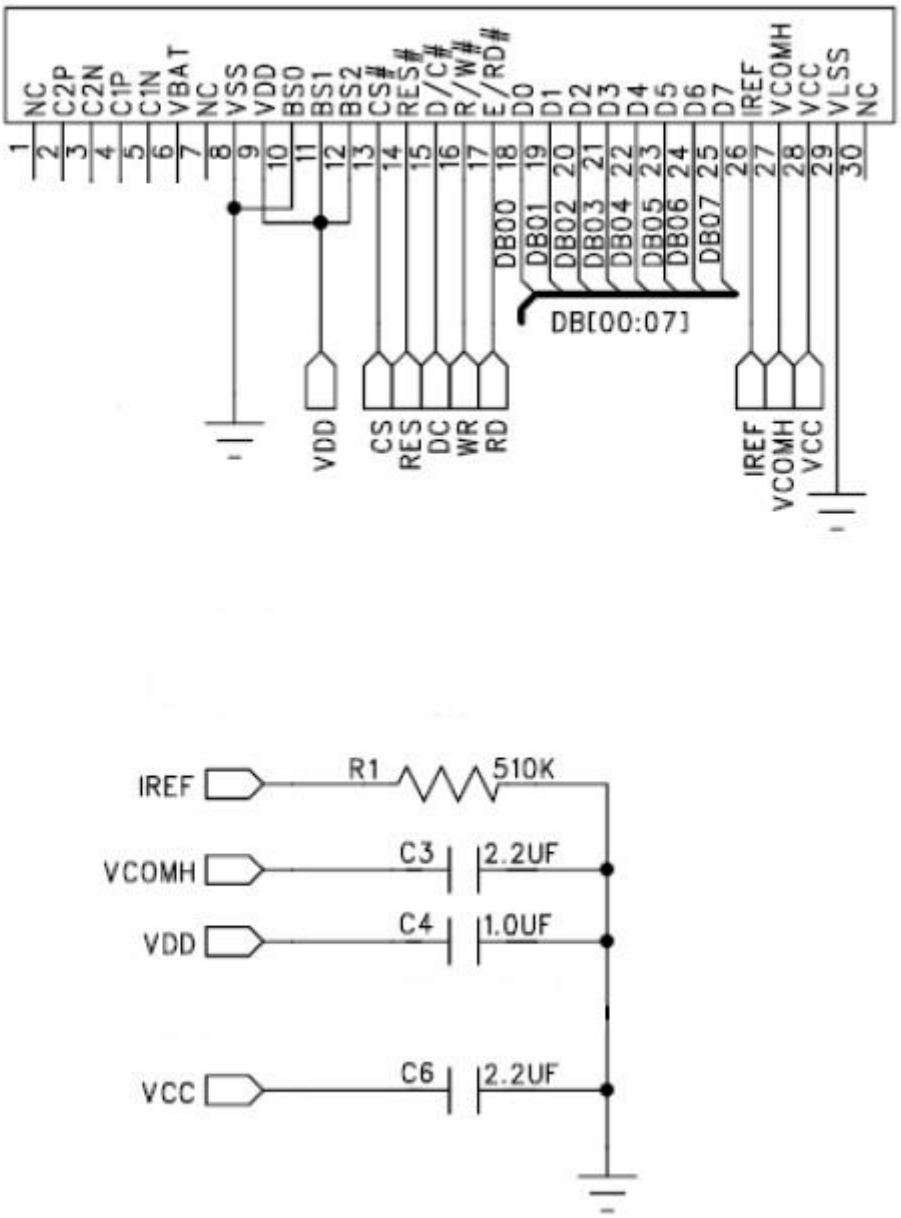
NOTE:

1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.

2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.

3. The VDD VBAT should be connected to external power supply.

◆8080 Series Interface Application Circuit(With External Charge Pump):



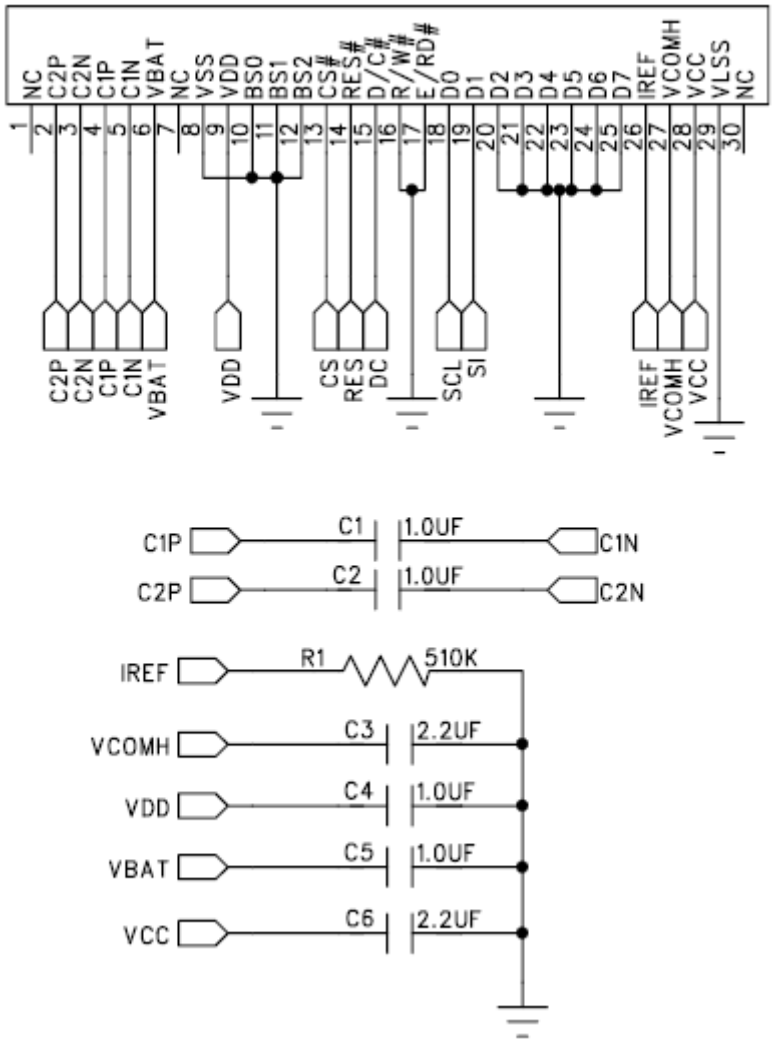
NOTE:

1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.

2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.

3. The VDD VCC should be connected to external power supply.

◆4-SPI Serial Interface Application Circuit(With Internal Charge Pump):



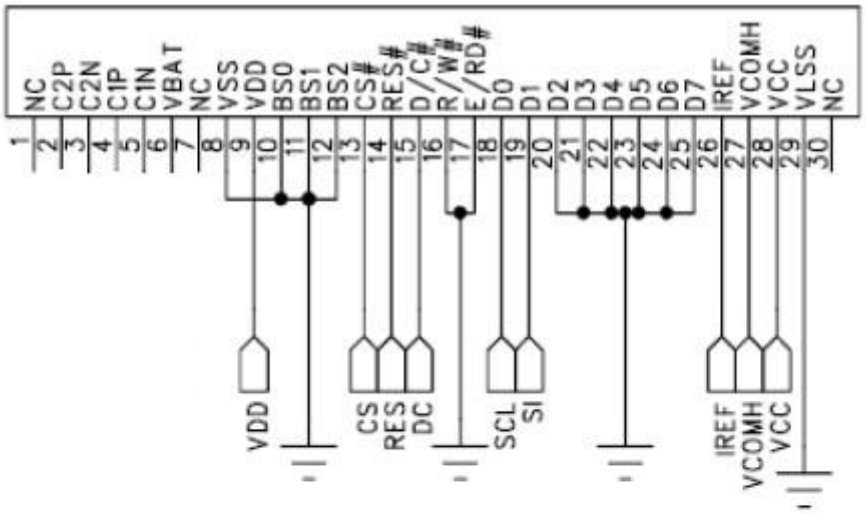
NOTE:

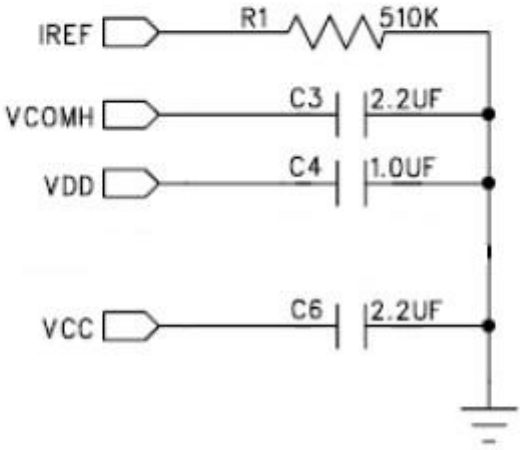
1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.

2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.

3. The VDD VBAT should be connected to external power supply.

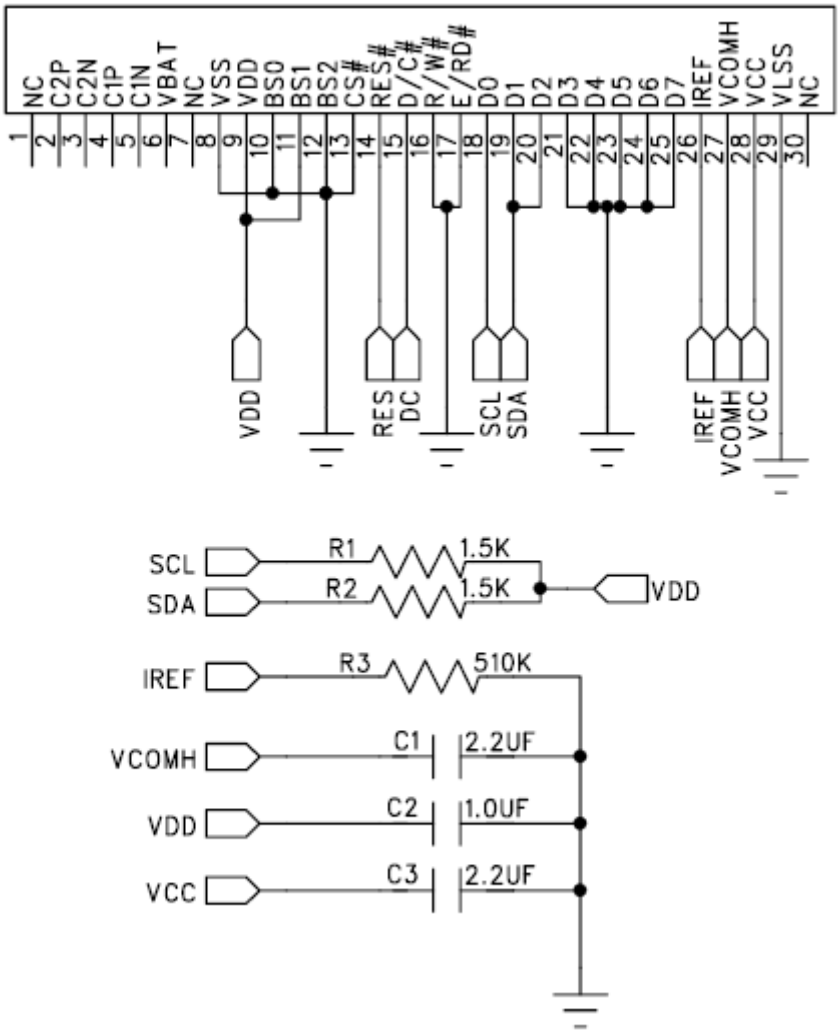
◆4-SPI Serial Interface Application Circuit(With External Charge Pump):





1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.
2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.
3. The VDD VCC should be connected to external power supply.

◆ IIC Interface Application Circuit (External Charge Pump):



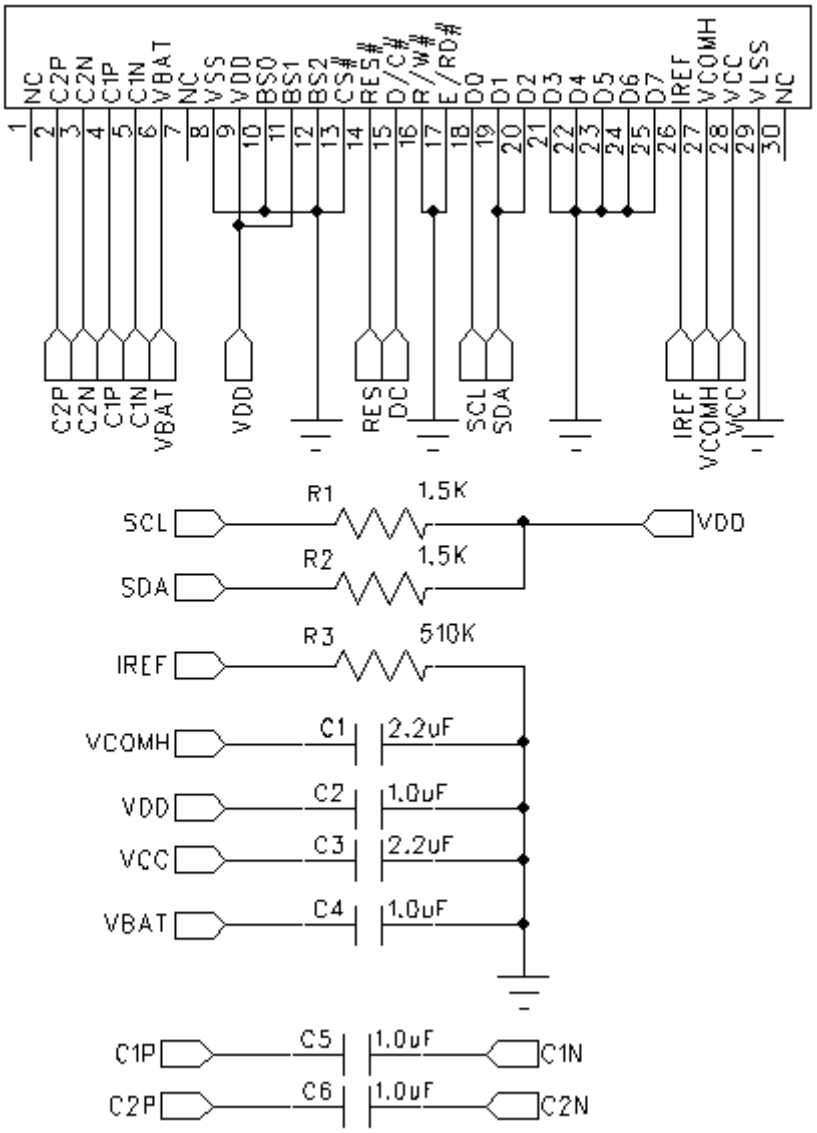
NOTE:

1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.

2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.

3. The VDD VCC should be connected to external power supply.

◆ IIC Interface Application Circuit (Internal Charge Pump):



NOTE:

1.The VCOMH capacitor is recommended to use tantalum capacitor to reduce noise.

2. The capacitor and the resistor value are recommended value. Select appropriate value against module application.

3. The VDD VBAT should be connected to external power supply.

■ RELIABILITY TESTS

<table>
<tr><th colspan="2">Item</th><th>Condition</th><th>Criterion</th></tr>
<tr><td colspan="2">High Temperature Storage
(HTS)</td><td>80±2℃, 200 hours</td><td rowspan="6">1. After testing, the function test is ok.
2. After testing, no addition to the defect.
3. After testing, the change of luminance should be within +/- 50% of initial value.
4. After testing, the change for the mono and area color must be within (+/-0.02, +/-0.02) and for the full color it must be within (+/-0.04, +/-0.04) of initial value based on 1931 CIE coordinates.
5. After testing, the change of total current consumption should be within +/- 50% of initial value.</td></tr>
<tr><td colspan="2">High Temperature Operating
(HTO)</td><td>70±2℃, 96 hours</td></tr>
<tr><td colspan="2">Low Temperature Storage
(LTS)</td><td>-30±2℃, 200 hours</td></tr>
<tr><td colspan="2">Low Temperature Operating
(LTO)</td><td>-20±2℃, 96 hours</td></tr>
<tr><td colspan="2">High Temperature / High Humidity Storage
(HTHHS)</td><td>50±3℃, 90%±3%RH, 120 hours</td></tr>
<tr><td colspan="2">Thermal Shock (Non-operation)
(TS)</td><td>-20±2℃ ~ 25℃ ~ 70±2℃
(30min) (5min) (30min)
10cycles</td></tr>
<tr><td>Vibration (Packing)</td><td>10~55~10Hz,amplitude 1.5mm, 1 hour for each direction x, y, z</td><td colspan="2" rowspan="2">1. One box for each test.
2. No addition to the cosmetic and the electrical defects.</td></tr>
<tr><td>Drop (Packing)</td><td>Height : 1 m, each time for 6 sides, 3 edges, 1 angle</td></tr>
<tr><td>ESD (finished product housing)</td><td>±4kV (R: 330Ω C: 150pF , 10times, air discharge)</td><td colspan="2">1. After testing, cosmetic and electrical defects should not happen.
2. In case of malfunction or defect caused by ESD damage, it would be judged as a good part if it would be recovered to normal state after resetting.</td></tr>
</table>

Note： 1) For each reliability test, the sample quantity is 3, and only for one test item.
2) The HTHHS test is requested the Pure Water(Resistance＞10MΩ).
3) The test should be done after 2 hours of recovery time in normal environment.

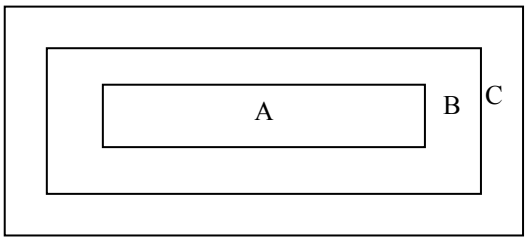
■ OUTGOING QUALITY CONTROL SPECIFICATION

◆Standard

According to GB/T2828.1-2003/ISO 2859-1：1999 and ANSI/ASQC Z1.4-1993, General Inspection Level II.

◆Definition

1 Major defect : The defect that greatly affect the usability of product.
2 Minor defect : The other defects, such as cosmetic defects, etc.
3 Definition of inspection zone:



Zone A: Active Area

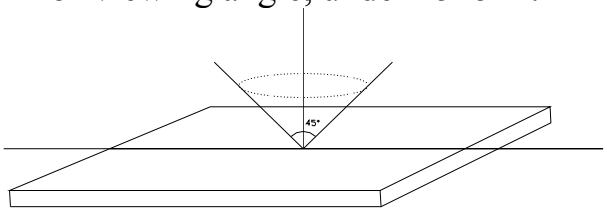
Zone B: Viewing Area except Zone A

Zone C: Outside Viewing Area

Note: As a general rule, visual defects in Zone C are permissible, when it is no trouble of quality and assembly to customer`s product.

◆Inspection Methods

1 The general inspection : under 20W x 2 or 40W fluorescent light, about 30cm viewing distance, within 45º viewing angle, under 25±5℃.



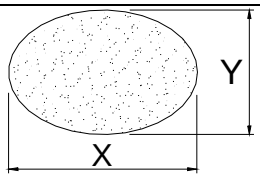
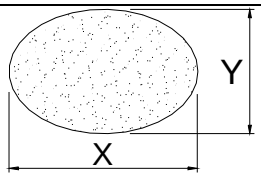
2 The luminance and color coordinate inspection : By PR705 or BM-7 or the equal equipments, in the dark room, under 25±5℃.

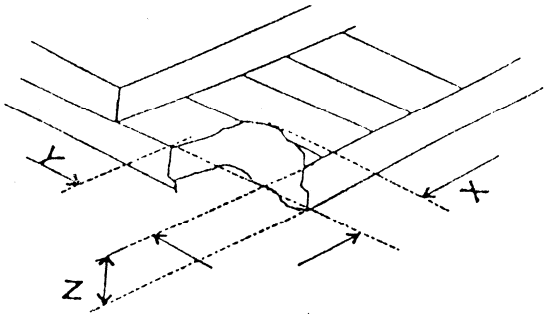
◆Inspection Criteria

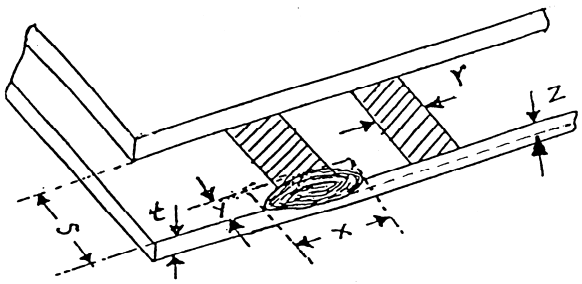
1 Major defect : AQL= 0.65

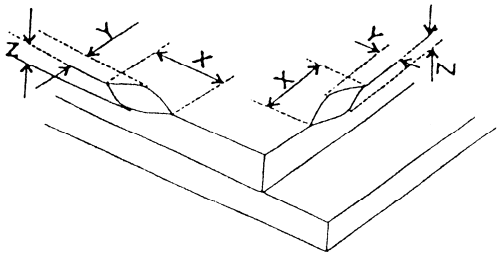
Item	Criterion
Function Defect	1. No display or abnormal display is not accepted
	2. Open or short is not accepted.
	3. Power consumption exceeding the spec is not accepted.
Outline Dimension	Outline dimension exceeding the spec is not accepted.
Glass Crack	Glass crack tends to enlarge is not accepted.

2 Minor Defect : AQL= 1.5

<table>
<tr><td>Item</td><td colspan="4">Criterion</td></tr>
<tr><td rowspan="5">Spot Defect (dimming and lighting spot)</td><td colspan="2" rowspan="2">Size (mm)</td><td colspan="2">Accepted Qty</td></tr>
<tr><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="3"> 
</td><td>Φ≦0.07</td><td colspan="2">Ignored</td></tr>
<tr><td>0.07＜Φ≦0.10</td><td>3</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.10＜Φ≦0. 15</td><td>1</td></tr>
<tr><td></td><td colspan="3">Note : Φ= (x + y) / 2</td><td>0.15＜Φ</td><td>0</td></tr>
<tr><td rowspan="5">Line Defect (dimming and lighting line)</td><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignored</td></tr>
<tr><td>L≦3.0</td><td>0.02＜W≦0.03</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>L≦2.0</td><td>0.03＜W≦0.05</td><td>1</td></tr>
<tr><td>/</td><td>0.05＜W</td><td>As spot defect</td></tr>
<tr><td colspan="5">Remarks: The total of spot defect and line defect shall not exceed 4 pcs. The distance between two lines defects must exceed 1 mm</td></tr>
<tr><td>Polarizer Stain</td><td colspan="4">Stain which can be wiped off lightly with a soft cloth or similar cleaning is accepted, otherwise, according to the Spot Defect and the Line Defect.</td></tr>
<tr><td rowspan="7">Polarizer Scratch</td><td colspan="4">1. If scratch can be seen during operation, according to the criterions of the Spot Defect and the Line Defect.</td></tr>
<tr><td colspan="4">2. If scratch can be seen only under non-operation or some special angle, the criterion is as below :</td></tr>
<tr><td>L (Length) : mm</td><td>W (Width) : mm</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td>/</td><td>W≦0.02</td><td colspan="2">Ignore</td></tr>
<tr><td>3.0＜L≦5.0</td><td>0.02＜W≦0.04</td><td>2</td><td rowspan="3">Ignore</td></tr>
<tr><td>L≦3.0</td><td>0.04＜W≦0.06</td><td>1</td></tr>
<tr><td>/</td><td>0.06＜W</td><td>0</td></tr>
<tr><td rowspan="5">Polarizer Air Bubble</td><td colspan="2">Size</td><td>Area A + Area B</td><td>Area C</td></tr>
<tr><td rowspan="4"> 
</td><td>Φ≦0.20</td><td colspan="2">Ignored</td></tr>
<tr><td>0.20＜Φ≦0.30</td><td>2</td><td rowspan="3">Ignored</td></tr>
<tr><td>0.30＜Φ≦0.50</td><td>1</td></tr>
<tr><td>0.50＜Φ</td><td>0</td></tr>
</table>

<table>
<tr><td rowspan="4">Glass Defect (Glass Chiped)</td><td>1. On the corner
(mm)
 

<table><tr><td>x</td><td>≤ 1.5</td></tr><tr><td>y</td><td>≤ 1.5</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>2. On the bonding edge
(mm)
 

<table><tr><td>x</td><td>≤ a / 4</td></tr><tr><td>y</td><td>≤ s / 3 &≤0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>3. On the other edges
(mm)
 

<table><tr><td>x</td><td>≤ a / 8</td></tr><tr><td>y</td><td>≤ 0.7</td></tr><tr><td>z</td><td>≤ t</td></tr></table></td></tr>
<tr><td>Note: t: glass thickness ; s: pad width ; a: the length of the edge</td></tr>
<tr><td>TCP Defect</td><td>Crack, deep fold and deep pressure mark on the TCP are not accepted</td></tr>
<tr><td>Pixel Size</td><td>The tolerance of display pixel dimension should be within ±20% of the spec</td></tr>
<tr><td>Luminance</td><td>Refer to the spec or the reference sample</td></tr>
<tr><td>Color</td><td>Refer to the spec or the reference sample</td></tr>
</table>

■ CAUTIONS IN USING OLED MODULE

◆Precautions For Handling OLED Module:

1. OLED module consists of glass and polarizer. Pay attention to the following items when handling:
   i. Avoid drop from high, avoid excessive impact and pressure.
   ii. Do not touch, push or rub the exposed polarizers with anything harder than an HB pencil lead.
   iii. If the surface becomes dirty, breathe on the surface and gently wipe it off with a soft dry cloth. If it is terrible dirty, moisten the soft cloth with Isopropyl alcohol or Ethyl alcohol. Other solvents may damage the polarizer. Especially water, Ketone and Aromatic solvents.
   iv. Wipe off saliva or water drops immediately, contact the polarizer with water over a long period of time may cause deformation.
   v. Please keep the temperature within specified range for use and storage. Polarization degradation, bubble generation or polarizer peeling-off may occur with high temperature and high humidity.
   vi. Condensation on the surface and the terminals due to cold or anything will damage, stain or dirty the polarizer, so make it clean as the way of iii.
2. Do not attempt to disassemble or process the OLED Module.
3. Make sure the TCP or the FPC of the Module is free of twisting, warping and distortion, do not pull or bend them forcefully, especially the soldering pins. On the other side, the SLIT part of the TCP is made to bend in the necessary case.
4. When assembling the module into other equipment, give the glass enough space to avoid excessive pressure on the glass, especially the glass cover which is much more fragile.
5. Be sure to keep the air pressure under 120 kPa, otherwise the glass cover is to be cracked.
6. Be careful to prevent damage by static electricity:
   i. Be sure to ground the body when handling the OLED Modules.
   ii. All machines and tools required for assembling, such as soldering irons, must be properly grounded.
   iii. Do not assemble and do no other work under dry conditions to reduce the amount of static electricity generated. A relative humidity of 50%-60% is recommended.
   iv. Peel off the protective film slowly to avoid the amount of static electricity generated.
   v. Avoid to touch the circuit, the soldering pins and the IC on the Module by the body.
   vi. Be sure to use anti-static package.
7. Contamination on terminals can cause an electrochemical reaction and corrade the terminal circuit, so make it clean anytime.
8. All terminals should be open, do not attach any conductor or semiconductor on the terminals.
9. When the logic circuit power is off, do not apply the input signals.
10. Power on sequence: $V_{DD} \rightarrow V_{CC}$, and power off sequence: $V_{CC} \rightarrow V_{DD}$.
11. Be sure to keep temperature, humidity and voltage within the ranges of the spec, otherwise shorten Module’ s life time, even make it damaged.
12. Be sure to drive the OLED Module following the Specification and datasheet of IC controller, otherwise something wrong may be seen.
13. When displaying images, keep them rolling, and avoid one fixed image displaying more

than 30 seconds, otherwise the residue image is to be seen. This is the speciality of OLED.

◆Precautions For Soldering OLED Module:

1. Soldering temperature : 260°C ± 10°C.
2. Soldering time : 3-4 sec.
3. Repeating time : no more than 3 times.
4. If soldering flux is used, be sure to remove any remaining flux after finishing soldering operation. (This does not apply in the case of a non-halogen type of flux.) It is recommended to protect the surface with a cover during soldering to prevent any damage due to flux spatters.

◆ Precautions For Storing OLED Module:

1. Be sure to store the OLED Module in the vacuum bag with dessicant.
2. If the Module can not be used up in 1 month after the bag being opened, make sure to seal the Module in the vacuum bag with dessicant again.
3. Store the Module in a dark place, do not expose to sunlight or fluorescent light.
4. The polarizer surface should not touch any other objects. It is recommended to store the Module in the shipping container.
5. It is recommended to keep the temperature between 0°C and 30°C , the relative humidity not over 60%.

◆ Limited Warranty

Unless relevant quality agreements signed with customer and law enforcement, for a period of 12 months from date of production, all products (except automotive products) TRULY will replace or repair any of its OLED modules which are found to be functional defect when inspected in accordance with TRULY OLED acceptance standards (copies available upon request). Cosmetic/visual defects must be returned to TRULY within 90 days of shipment. Confirmation of such date should be based on freight documents. The warranty liability of TRULY is limited to repair and/or replacement on the terms above. TRULY will not be responsible for any subsequent or consequential events.

◆Return OLED Module Under Warranty:

1. No warranty in the case that the precautions are disregarded.
2. Module repairs will be invoiced to the customer upon mutual agreement. Modules must be returned with sufficient description of the failures or defects.

◆PRIOR CONSULT MATTER

1. For TRULY standard products , we keep the right to change material ,process … for improving the product property without any notice on our customer.
2. If you have special requirement about reliability condition, please let us know before you start the test on our samples.